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Concept for a Power System Controller for Large Space Electrical Power Systems

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National Aeronautics
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TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

TECHNICAL PAPER

CONCEPT FOR A POWER SYSTEM CONTROLLER FOR LARGE SPACE ELECTRICAL POWER SYSTEMS

INTRODUCTION

As a result of the Skylab and 25 kW Power Module programs, a need for autonomous control of large space electrical power systems has emerged. Autonomous control implies the need for a device or devices which will make system level decisions and take the necessary action(s) required to implement the decision(s) correctly and quickly without a man-machine interface. Therefore, a Marshall Space Flight Center Director's Discretionary Fund task was undertaken to develop technology for a fail-operational Power System Controller (PSC) utilizing microprocessor technology for managing the distribution and power processor subsystems of a large multi-kW space Electrical Power System (EPS). The task involved determining the specific functions which must be performed by the PSC to enable autonomous EPS operation, determining the best microprocessor available to do the job, and determining the feasibility, cost savings and applications of a PSC. Finally, a limited function breadboard version of a PSC was developed to demonstrate the concept and the potential cost savings of a power system containing a PSC. The results of this task are discussed in this paper.

PSC TASKS

The primary functions of a PSC are to monitor the status of the Electrical Power and Distribution System (EPDS) (Fig. 1), make system level computations and decisions, and to initiate required system actions by appropriate commands to the various distribution and processing components, such as relays, remote power controllers, remote control circuit breakers, and programmable power processors (P^3). A total of eight specific functions are required of the PSC to enable autonomous EPS operation. They are as follows:

1) Provide a single point interface between the spacecraft and the power system. In the case of the 25 kW Power Module, used as a basis for this study, this involves providing an interface between the P^3's and distribution components and the remote interface unit (RIU) of the spacecraft command and data handling (C&DH) system.

2) Update subsystem parameters as required for proper management and control of the EPS. This includes updating voltage and current parameters of individual solar arrays, batteries, power processors, and buses, either from information located in a storage device, such as a P^3, or sensing these values directly and storing them in the PSC's memory.

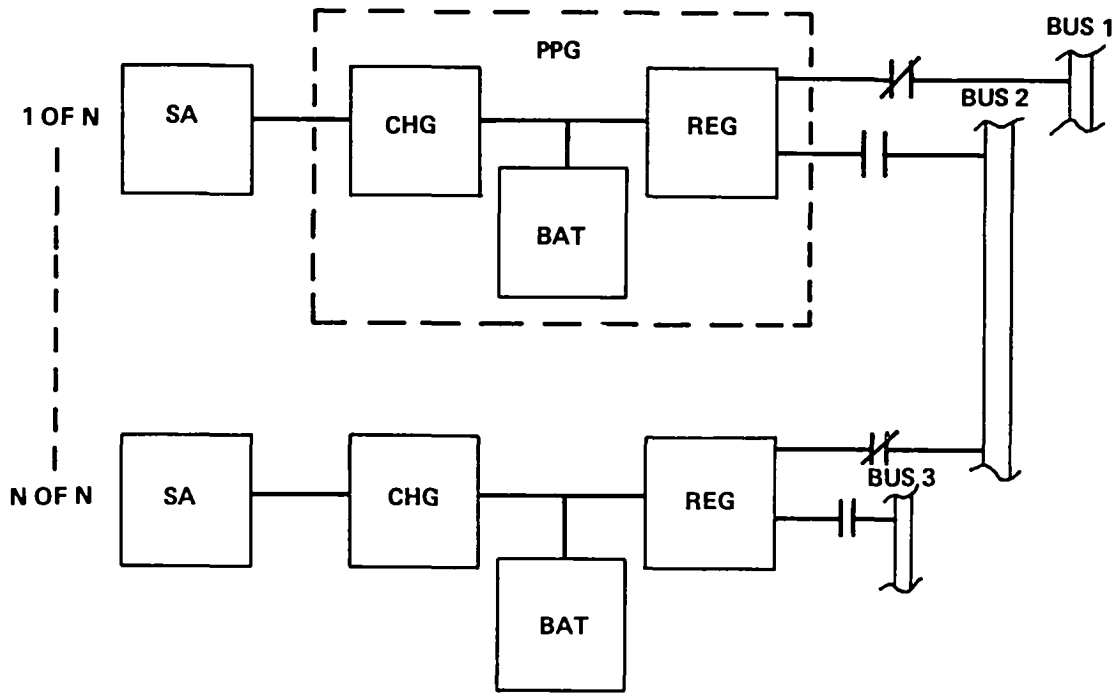

Figure 1. Typical electrical power and distribution system.

3) Detect EPS faults and take corrective action by load reassignment and/or load shedding. For example, in a power system with multiple channels, this would involve detecting a faulted channel, removing it from the load bus, and then, based on system capability, either shedding loads or re-configuring loads such that they are shared equally by the remaining channels.

4) Predict load requirements and system capabilities to determine priorities and sequences of experiment operations to maximize use of available power and experiment hardware. This involves real-time load management or pre-determined load sequences which are programmed in the PSC memory prior to launch.

5) Detect system degradation and implement corrective action. This involves monitoring the key components of the power system, determining the degree of degradation, and at some point, reducing the degraded elements load, switching to a redundant element, or removing the element from service.

6) Implement periodic maintenance procedures to lengthen the life of the system. An example of this is battery reconditioning which results in extended battery lifetime with dependable, useable capacity.

7) Adjust subsystem parameters automatically or from ground commands. This requires sensing subsystem parameters and implementing required parameter changes based on internal calculations or ground commands.

8) Perform a redundant configuration to assure fail-operational capability.

Implementation of these eight functions is feasible with the present EPDS and PSC state-of-the-art technology. However, as technology advances are made and space power systems become even more complicated, this list could grow. Therefore, a PSC should be versatile enough to accommodate additional capabilities in the future.

MICROPROCESSOR COMPARISONS

PSC requirements dictate the use of a fast, powerful central processing unit (CPU). The CPU must be able to perform numerous string operations, to handle multiple input/output functions with interrupts and to perform multiplication and division functions quickly. As a result, two new state-of-the-art 16-bit microprocessors, the ZILOG Z8000 and the INTEL 8086, were considered and compared in their abilities to perform the necessary functions required of the PSC.

The Z8000 microprocessor is a register-oriented CPU from Zilog with well-organized minicomputer-like architecture. Sixteen general-purpose registers, each two-bytes (one 16-bit word) wide, are available to the user. Over 100 instructions, and 400 combinations of instructions can be used to manipulate data between the CPU registers, memory and I/O [1].

The 8086 is a third generation CPU from Intel which is seven to ten times more powerful than the second generation 8080A. The standard operating speed of the 8086 CPU is 5 MHz (200 nanosecond cycle time) with a selected 8 MHz version also available. Up to 1 megabyte of memory can be addressed, along with a separate 65K I/O spare. The CPU has a complement of eight 16-bit general registers. These registers are subdivided into two sets of four registers each: the data registers, and the pointer and index registers. In addition, there are four segment registers used to manipulate large (64K) segments of memory. The 8086 has a repertory of about 100 assembled language instructions which can be combined to produce about 300 machine-level instructions [2].

Because of the new technology involved with both of these CPU's, complete support for the devices is difficult to obtain. Using a single board evaluation kit for each of the CPU's, a comparison was completed with the 8086 CPU used as a baseline for the PSC software. This was necessary as a result of the lack of Z8000 support at the present time.

The baselined program contained three major operations. These were: (1) I/O operations to five different devices; (2) string messages and string manipulating; and (3) moving data into and out of memory. In the 8086 CPU all I/O operations have to use two fixed registers. One register contains the address of the I/O port and the other contains the data to be input or output. This limits the programmer since there are a limited number of registers. The Z8000 CPU can input or output data through any of its 16 registers with the I/O port being addressed directly. As a result one Z8000 instruction is equivalent to three 8086 instructions in addition to the programmer being able to designate his own register for I/O operations in the Z8000 CPU. In performing string manipulations, the 8086 CPU requires approximately 15 instructions to output a known fixed length message. To accomplish the same operation in the Z8000 CPU requires approximately 10 instructions. Finally, because of the limited number of general purpose registers in the 8086 CPU, memory has

to be addressed for temporary storage of data, thus requiring more processing time and more memory space. In each of these three areas, the 8086 CPU requires more instructions to do the given job. This results in slower execution time and higher cost due to the longer programs.

PSC FOR THE 25 kW POWER MODULE EPS BREADBOARD

To demonstrate the PSC concept, a limited function PSC was designed for installation in the 25 kW Power Module EPS Breadboard (Fig. 2). As previously noted, the 8086 microprocessor was used as the baseline CPU for this PSC. The test PSC consists of an Intel MCS-86 system design kit, the SDK-86, a printed circuit (PC) board with the I/O devices and their associated logic, and the PSC software. This breadboard PSC samples data from the four P^3's in the 25 kW Power Module Breadboard, stores the data in its memory, and then outputs the data to a teletype on request.

The hardware for the PSC consists of two items, Intel's SDK-86 and the I/O PC board. The SDK-86 (Fig. 3) consists of the 8086 CPU with a clock frequency of 5 MHz, 8 K bytes of PROM memory, 2 K bytes of RAM memory, and the data bus, address bus and control bus buffering needed to fan out from the board. The I/O PC board (Fig. 4) consists of five programmable communication interface integrated circuits (8251A) and the logic and buffering required to "talk" to the correct device. As a system (Fig. 5), data from any of the four P^3's may be requested from the teletype, thus simplifying P^3 monitoring.

The software for the PSC consists of initialization, repeated sampling, and an interrupt driven output to the teletype. The general flowchart for the software is shown in Figure 6. The initialization routine consists of programming the five 8251A's and then sending a prompt to each P^3 to verify correct operation (the program assumes that the four P^3's are turned on). If there is a problem, a "Q" is sent back to the teletype informing the user that a problem has occurred. Next, the program samples each P^3 and retrieves the required data needed to maintain operation of the system. To obtain this data, the user types a C1, R1, C2, or R2 which stands for Charger 1, Regulator 1, Charger 2, or Regulator 2, respectively. After display the program returns to the sample loop.

PSC EXTRAPOLATION TO A 25 kW POWER MODULE EPS

Using the 25 kW Power Module Phase A EPS concept, a preliminary cost study was conducted to determine the potential cost savings which could be realized by using a PSC. The Phase A concept with twenty-four P^3's (12 chargers and 12 regulators) required five RIU's to interface with the C&DH system. At a cost of $250K for each RIU, the potential cost savings to be achieved by reducing the number of RIU's required is considerable and very real.

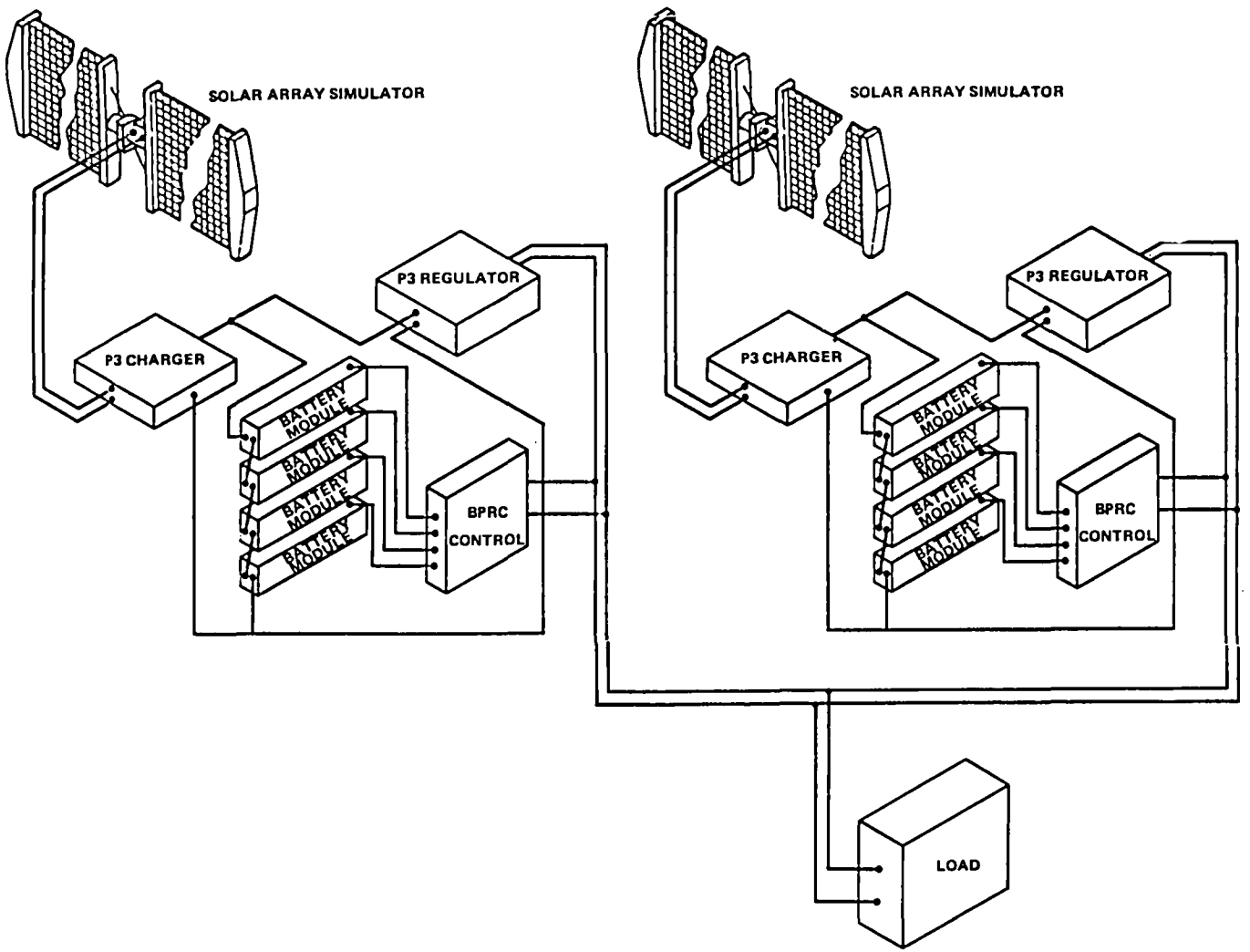

Figure 2. 25 kW Power Module breadboard.

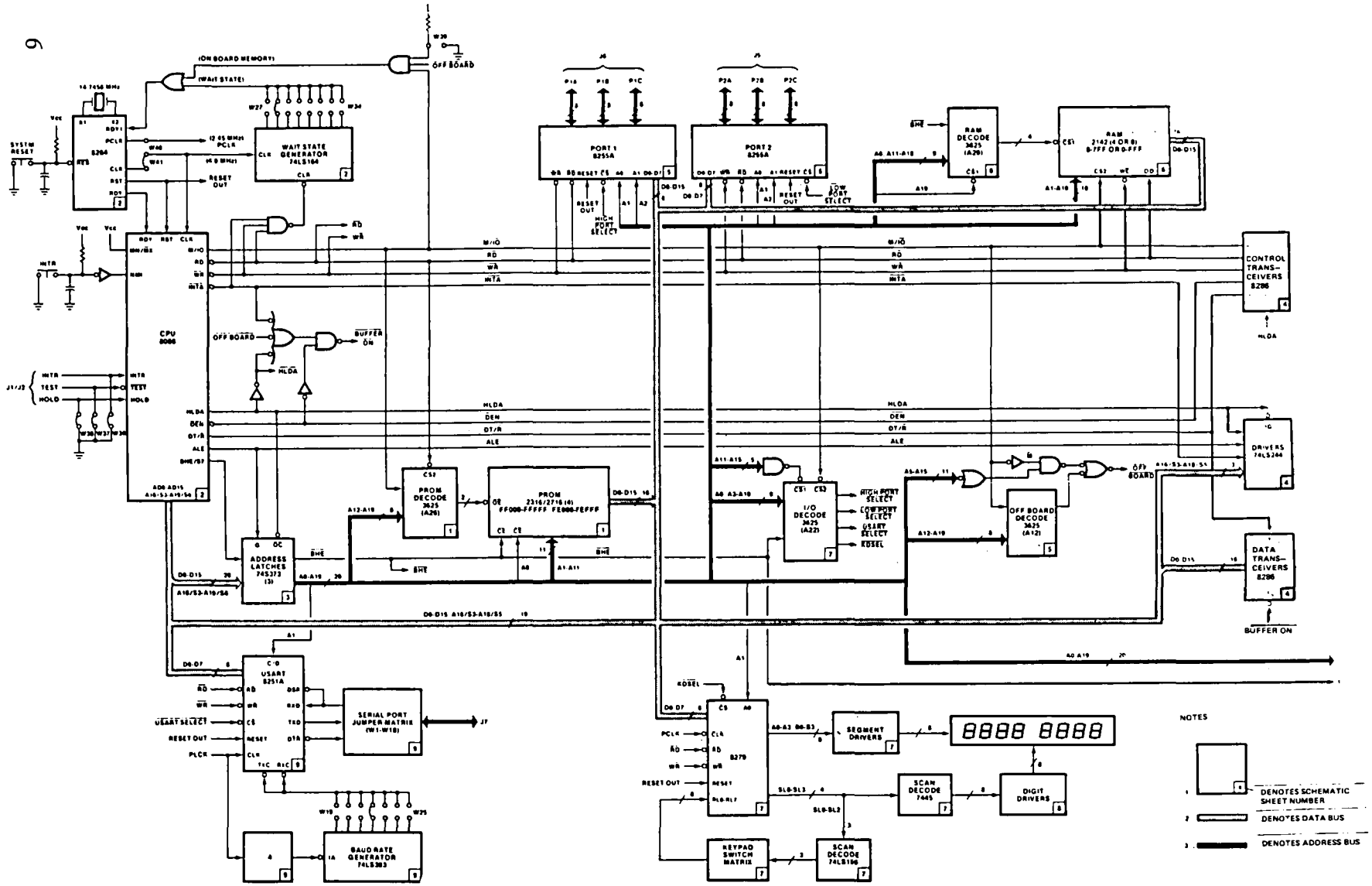

Figure 3. SDK-86 system design kit.

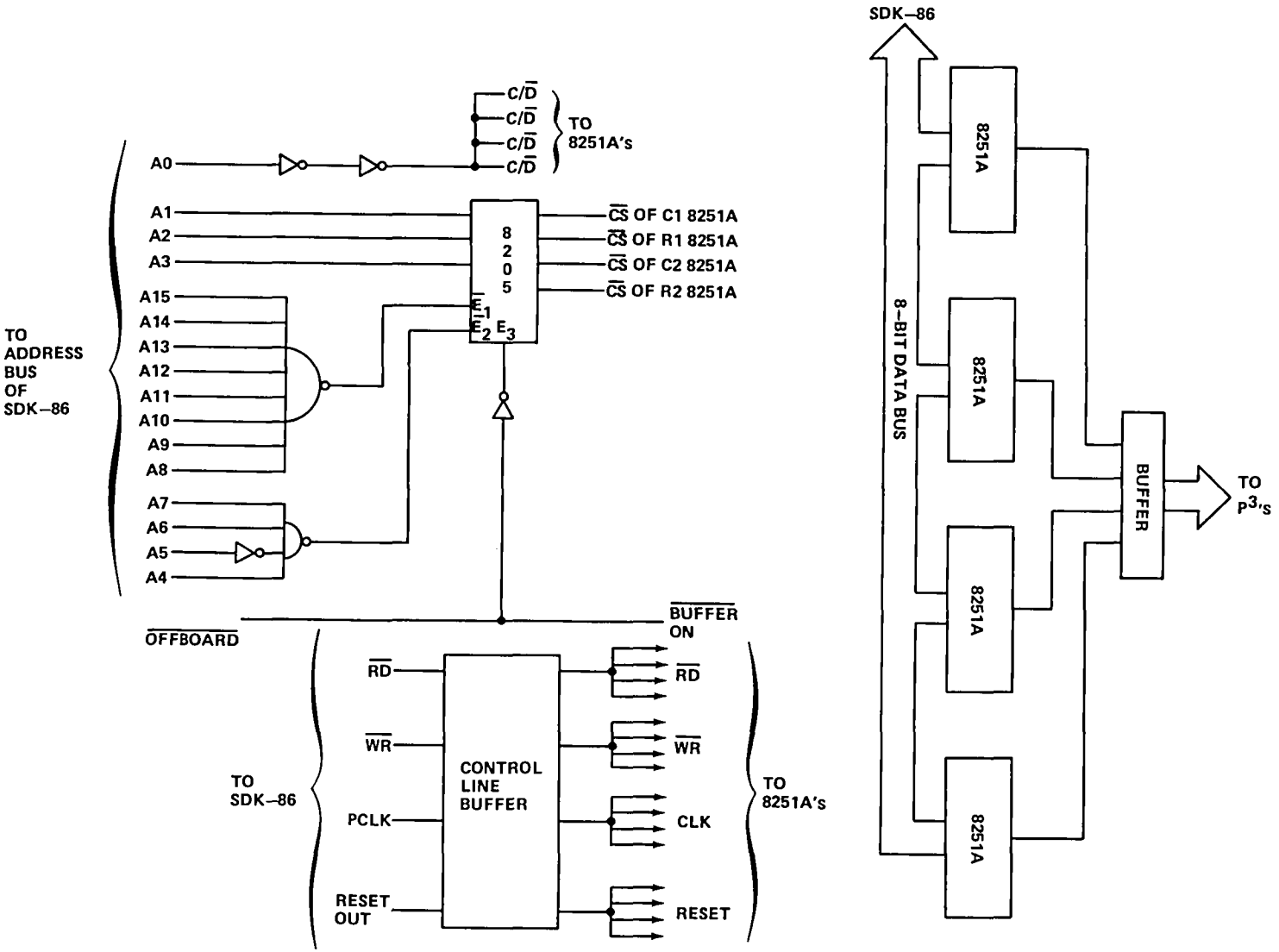

Figure 4. I/O board.

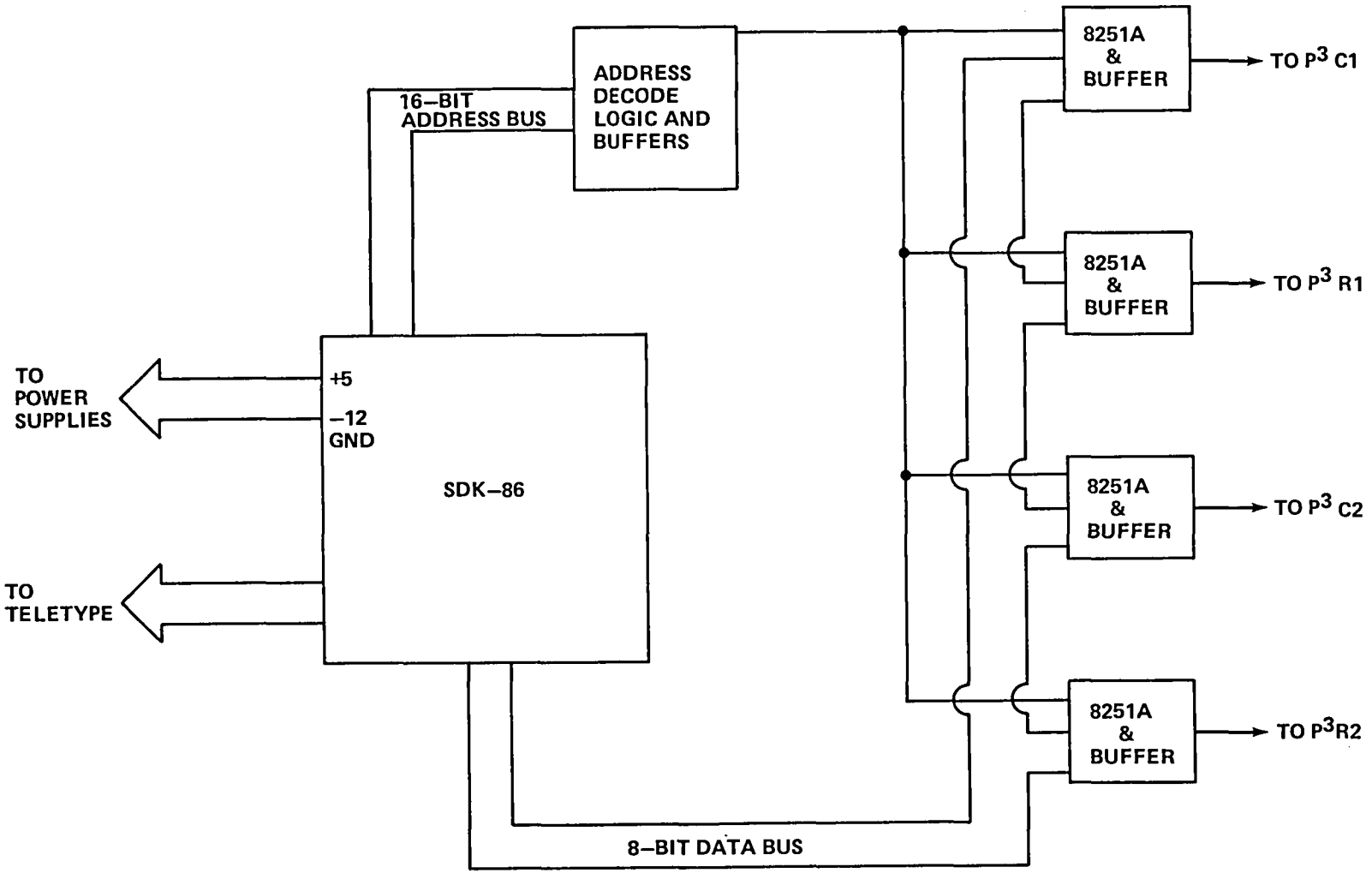

Figure 5. PSC breadboard.

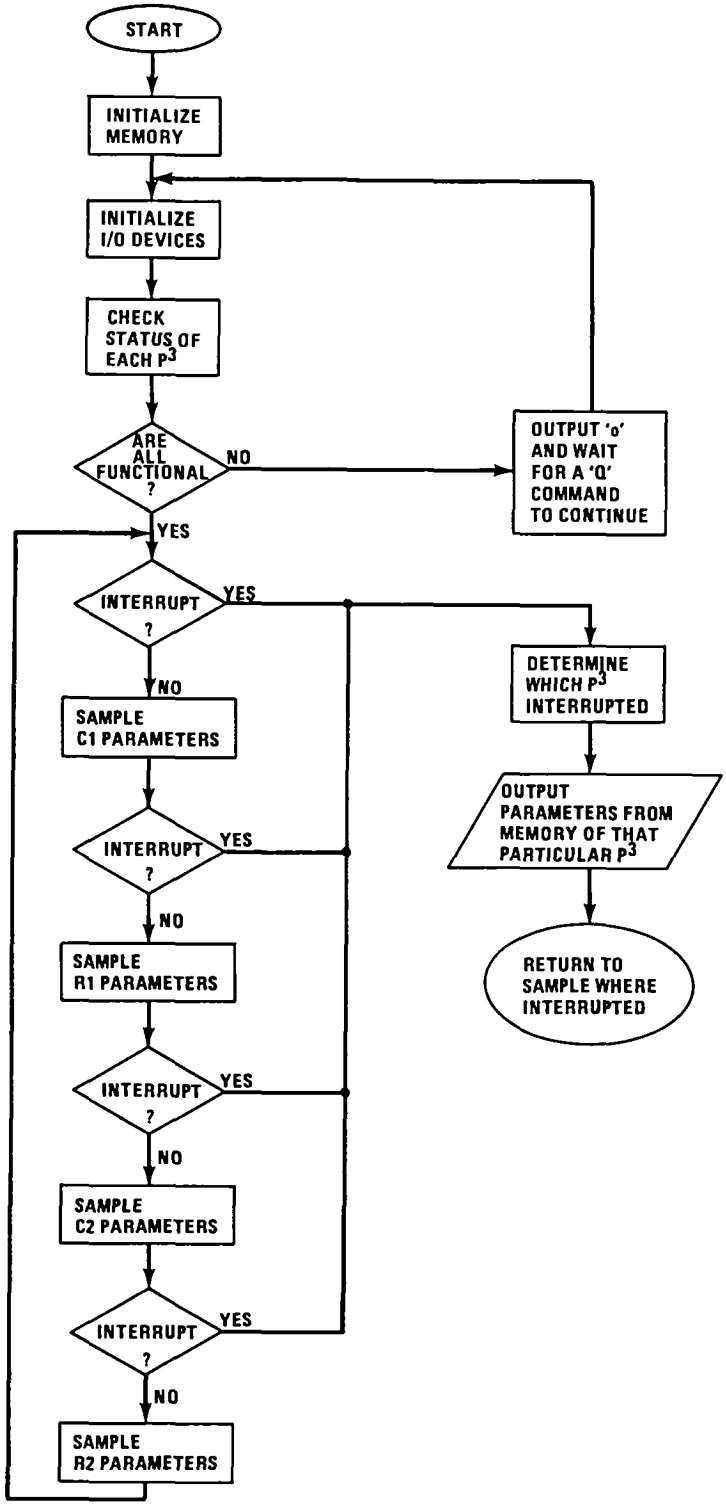

Figure 6. General flowchart.

Using the breadboard PSC data as a baseline, a study of the feasibility of using one PSC to talk to 24 P^3's and to interface with one RIU was made. Starting with the software, it was necessary to determine whether the 8086 CPU could sample the needed parameters of the 24 P^3's fast enough to meet the EPS data requirement of 10 samples/second. Using the 5 MHz clock cycle time of 8086 CPU, an estimation was made of the calculation times required for certain functions. For sampling four P^3's and then storing this data in memory, it takes approximately 42 microseconds to initialize the PSC, 4.25 milliseconds to sample a charger, and about 2.66 milliseconds to sample a regulator. Expanding this to a system composed of 12 P^3 chargers and 12 P^3 regulators, it would take approximately 0.21 milliseconds for initialization, 51 milliseconds to sample the chargers, and 32 milliseconds to sample the regulators. This totals to an approximate time of 83.21 milliseconds which is below the 100 millisecond minimum requirement.

Again, using the breadboard PSC software as a baseline, the following estimates of manpower and cost for an in-house design were made:

Packaging Design	0.5 Man Year
Quality Control	0.25 Man Year
Testing	0.25 Man Year
Software (3000 lines of assembly line code)	0.75 Man Year
Hardware (piece parts & packaging)	$10K

Thus, a total non-recurring development cost of less than 2.0 man years and a recurring cost of approximately $10K would be required for a PSC. This would result in savings of approximately $750K on the 25 kW Power Module, even with a redundant PSC and RIU used.

CONCLUSIONS

This effort, performed using the Center Director's Discretionary Funds, has demonstrated the viability and the potential for sizeable cost savings by using the PSC concept in large space electrical power systems. This was the goal of the task. Plans for the future include expanding the hardware and software to demonstrate additional capabilities in the 25 kW Power Module Breadboard, continued evaluation of the Z8000 CPU, and incorporation of the concepts developed in a technology program for autonomously managed multihundred kilowatt space power systems. Anticipations are that as technology increases in the area of smaller, more powerful microcomputers and power control devices, future large space power systems will require less, rather than more, ground surveillance and support. This will result in ever increasing cost savings and increased productivity of operation in space.

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2. The 8086 Family User's Manual; Intel Corporation, Literature Department, 3065 Bowers Avenue, Santa Clara, CA 95051; October 1979.

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16. ABSTRACT

A need for autonomous control of large electrical power systems has emerged. A Marshall Space Flight Center Director's Discretionary Fund task is undertaken to develop technology for a fail-operational Power System Controller (PSC) utilizing microprocessor technology for managing the distribution and power processor subsystems of a large multi-kW space Electrical Power System. The task involved determining the specific functions which must be performed by the PSC, determining the best microprocessor available to do the job, and determining the feasibility, cost savings, and applications of a PSC. A limited function breadboard version of a PSC was developed to demonstrate the concept and potential cost savings.

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